

APPROVED	O.G. FIG. 1	
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FIG. 1

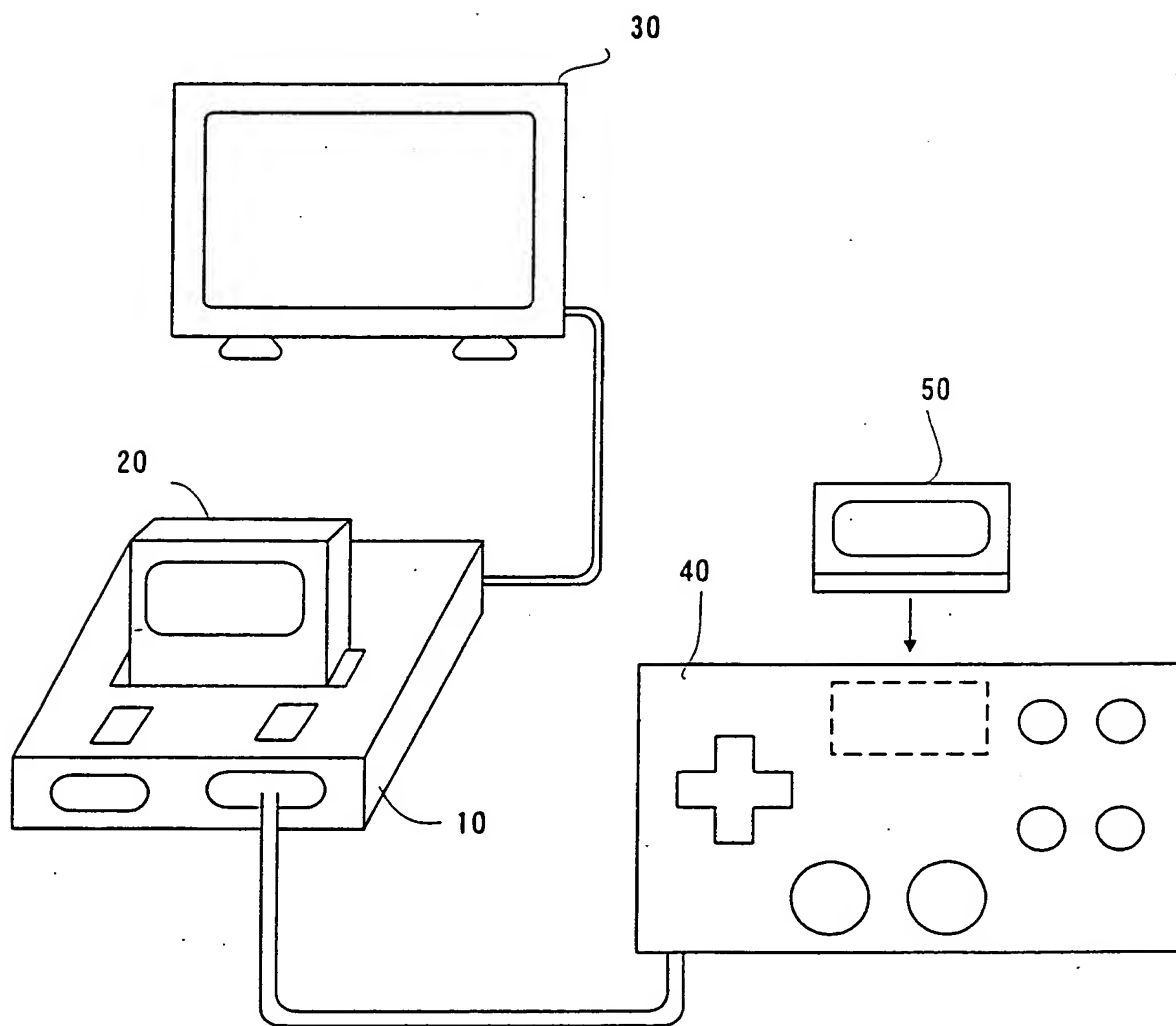
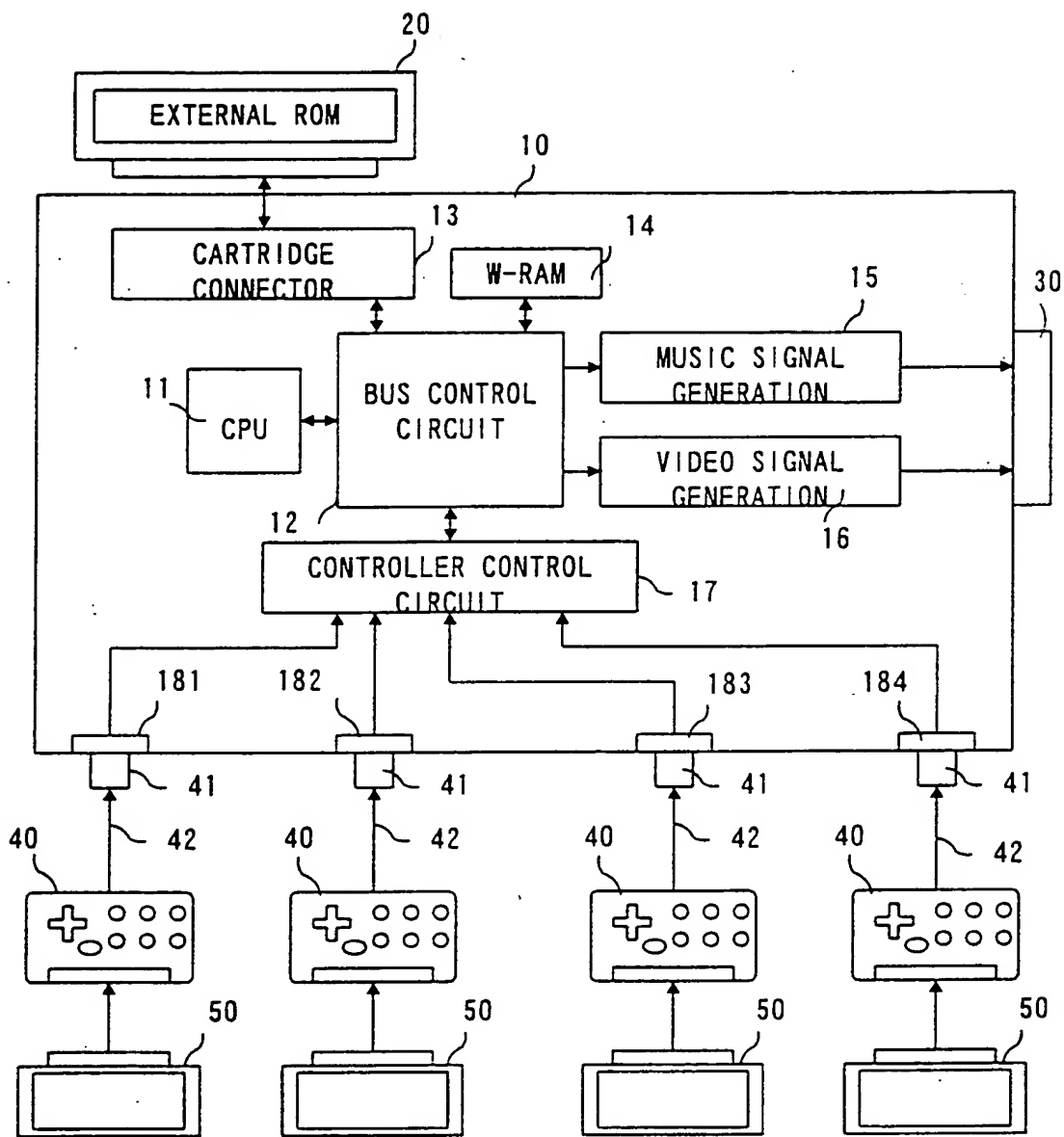


FIG. 2



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FIG. 3

CPU MEMORY MAP

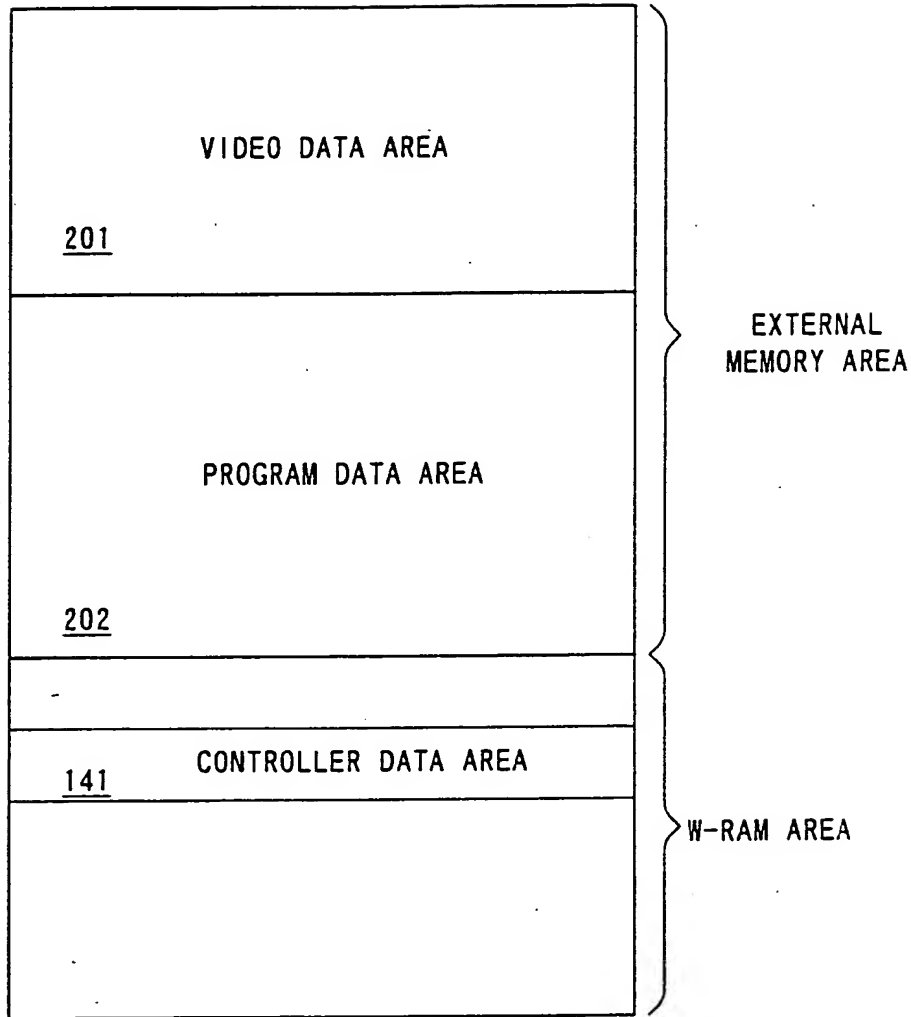
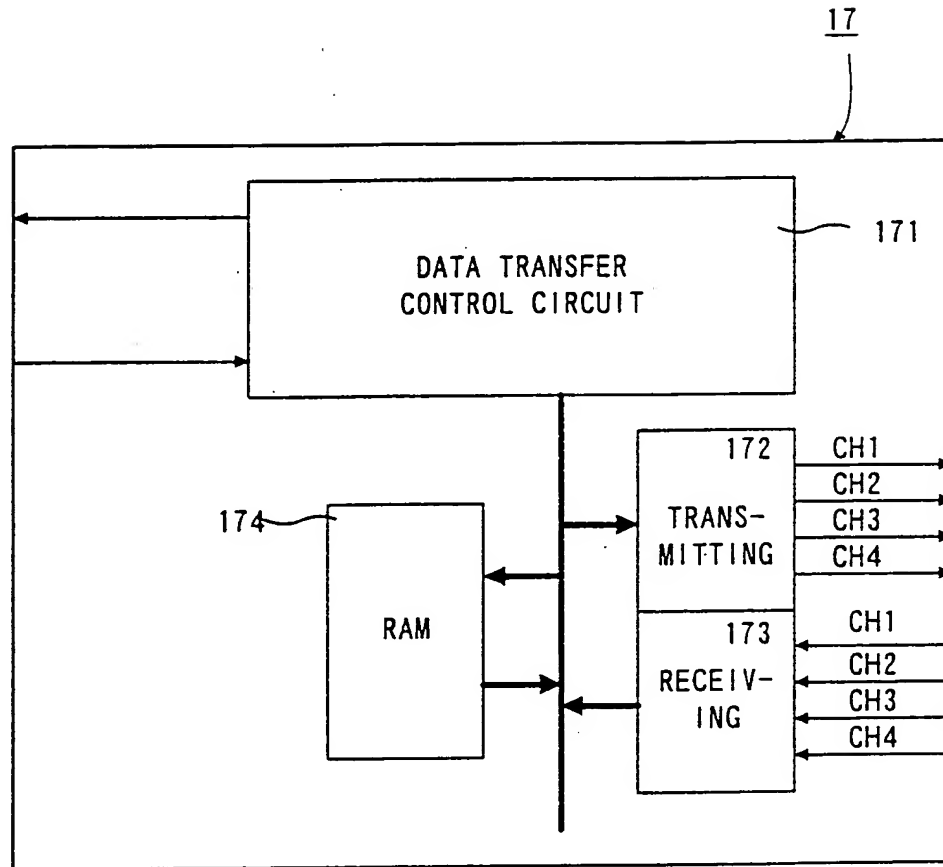


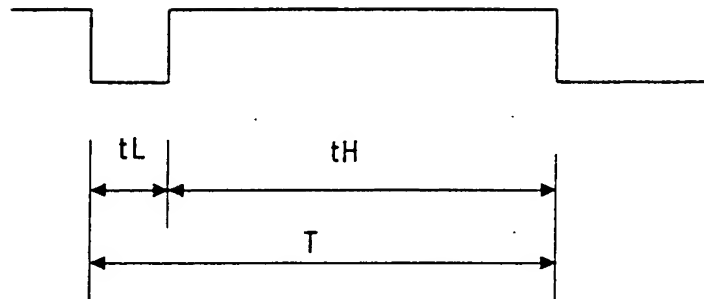
FIG. 4



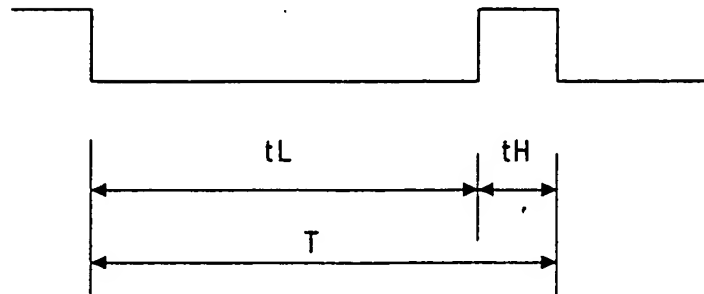
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FIG. 5

[1] SIGNAL



[0] SIGNAL



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FIG. 6

RAM 174

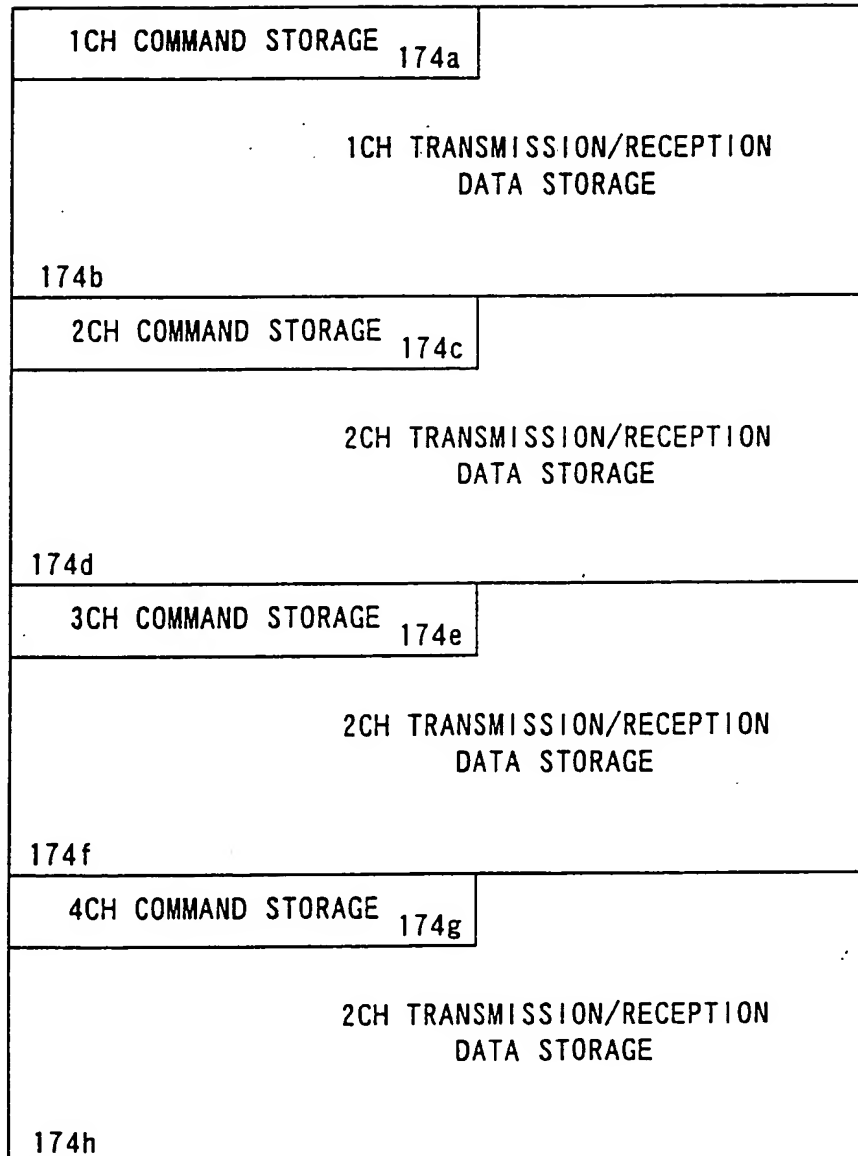


FIG. 7

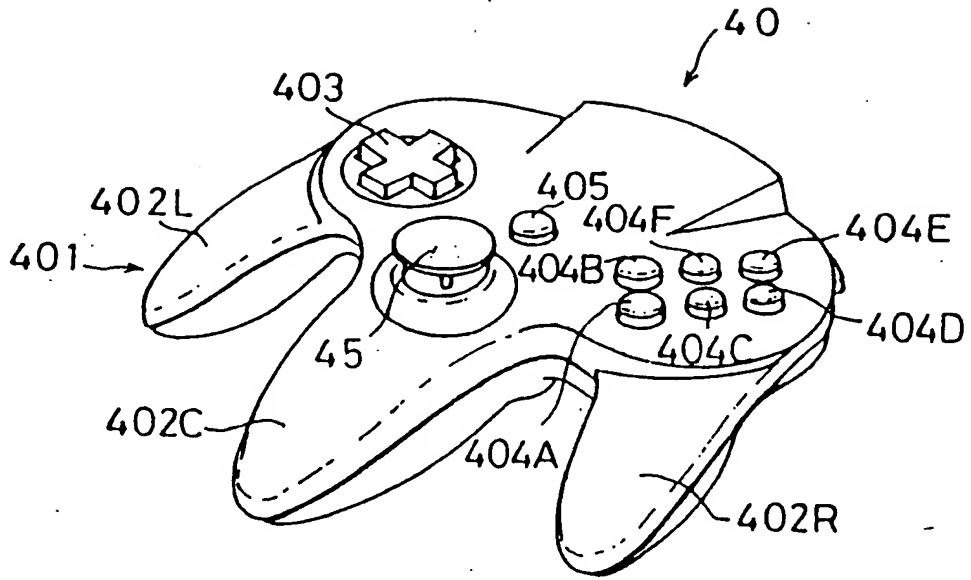


FIG. 8

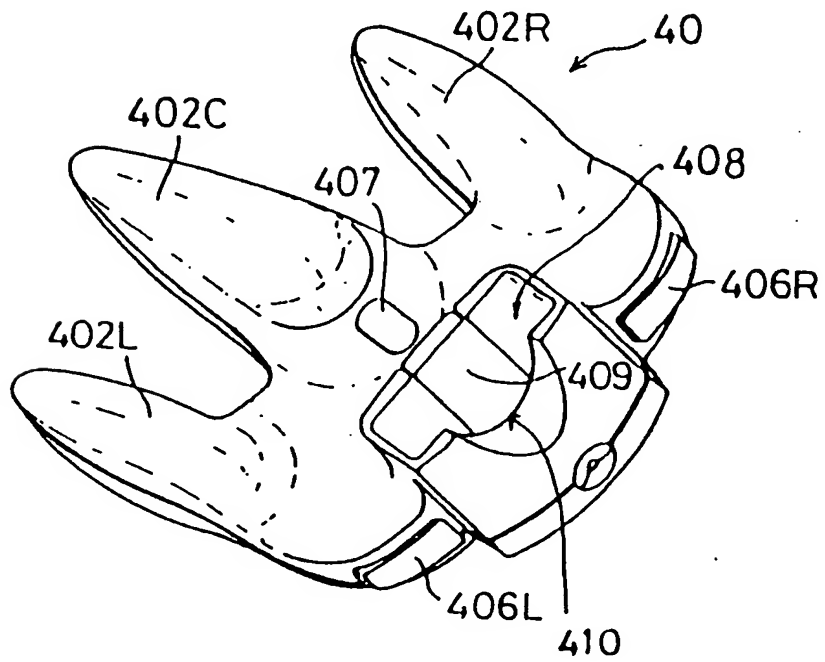
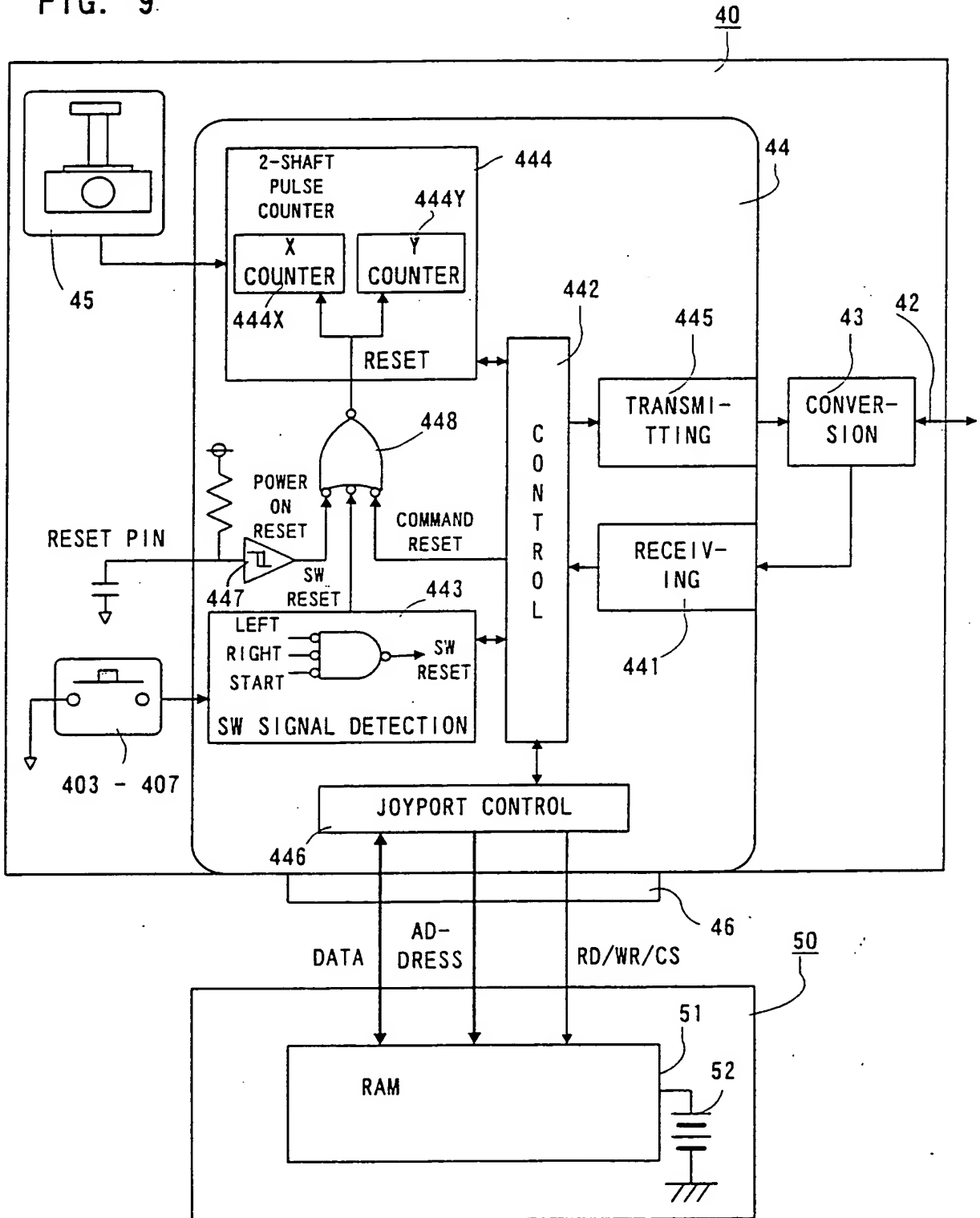


FIG. 9







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FIG. 11

COMMAND 0: TRANSMITTING TYPE OF COMMAND  
RECEPTION: 1 BYTE TRANSMISSION: 3 BYTES

		d7	d6	d5	d4	d3	d2	d1	d0
RECEP- TION	1 BYTE	COMMAND 0							
	1 BYTE	TYPE L							
TRANS- MISSION	2 BYTE	TYPE H							
	3 BYTE	STATUS							

FIG. 12

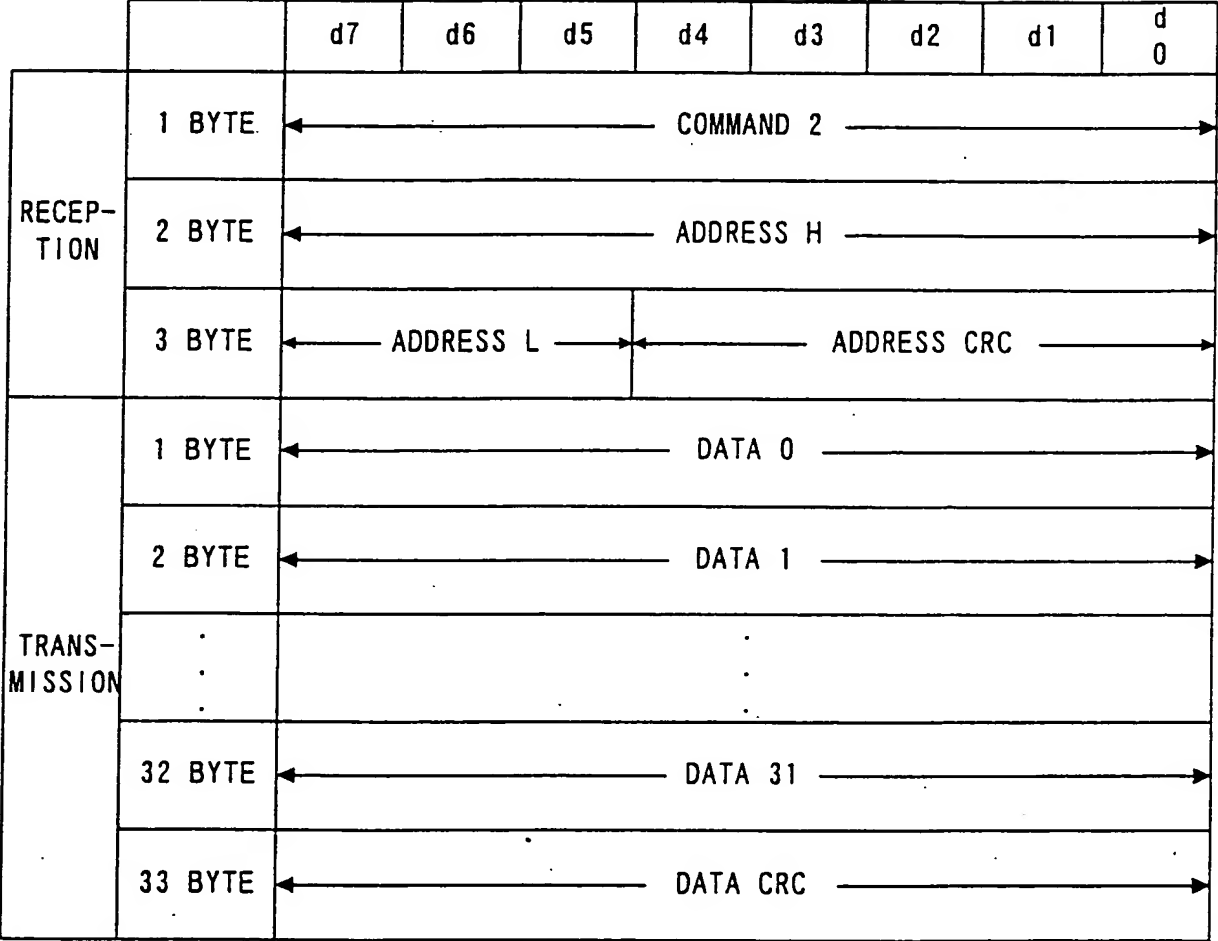
COMMAND 1: ACCESSING STANDARD CONTROLLER  
RECEPTION: 1 BYTE TRANSMISSION: 4 BYTES

		d7	d6	d5	d4	d3	d2	d1	d0
RECEP- TION	1 BYTE	COMMAND 1							
	1 BYTE	B	A	G	START	↑	↓	←	→
TRANS- MISSION	2 BYTE	JSRST*	0	L	R	E	D	C	F
	3 BYTE	X ORDINATE							
	4 BYTE	Y ORDINATE							

\* HIGH LEVEL AT TIME THAT L,R, START BUTTONS ARE  
SIMULTANEOUSLY DEPRESSED

FIG. 13

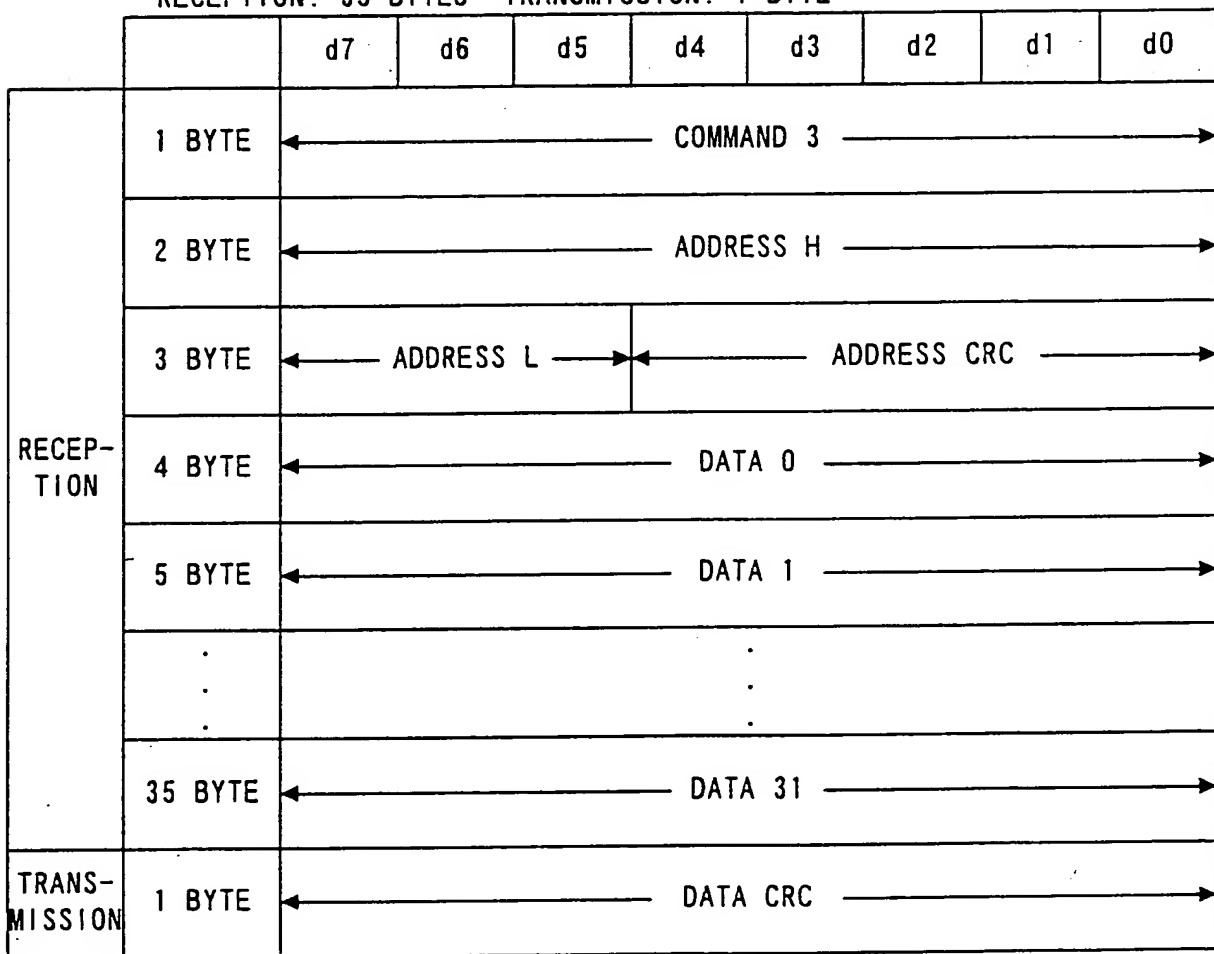
COMMAND 2:      READ-OUT RAM  
RECEPTION: 3 BYTES    TRANSMISSION: 33 BYTES



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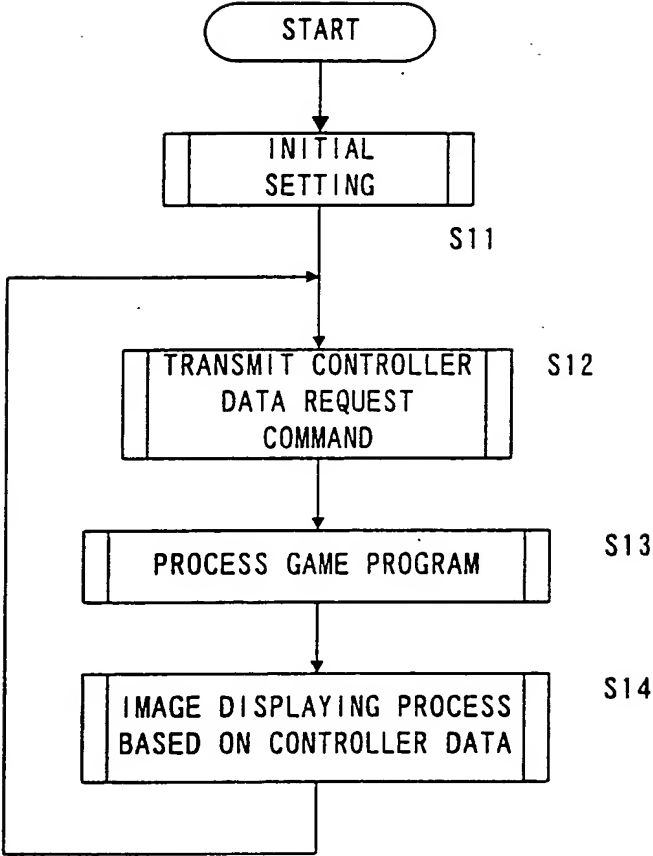
FIG. 14

COMMAND 3: WRITING INTO RAM  
 RECEPTION: 35 BYTES TRANSMISSION: 1 BYTE



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FIG. 15



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FIG. 16

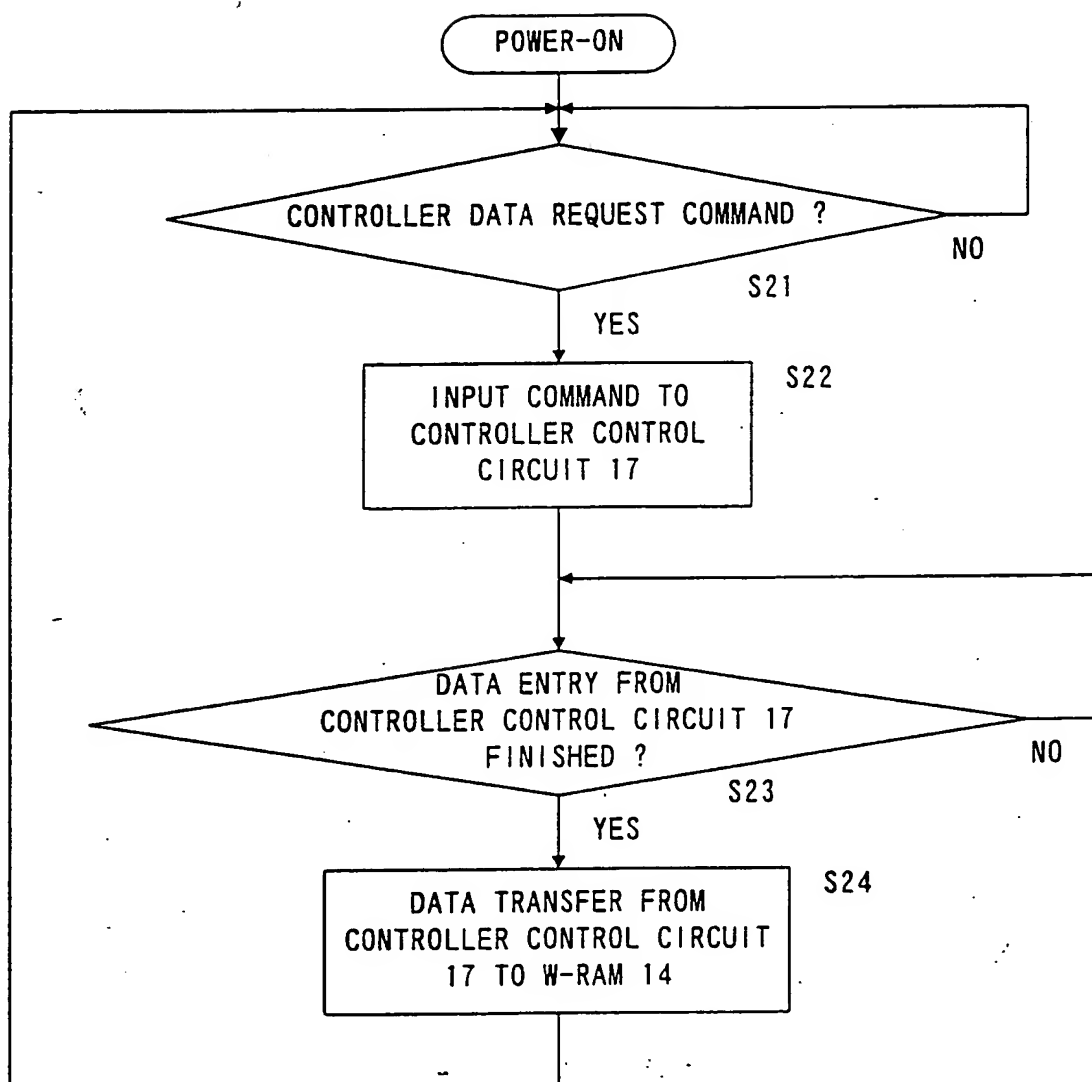


FIG. 17

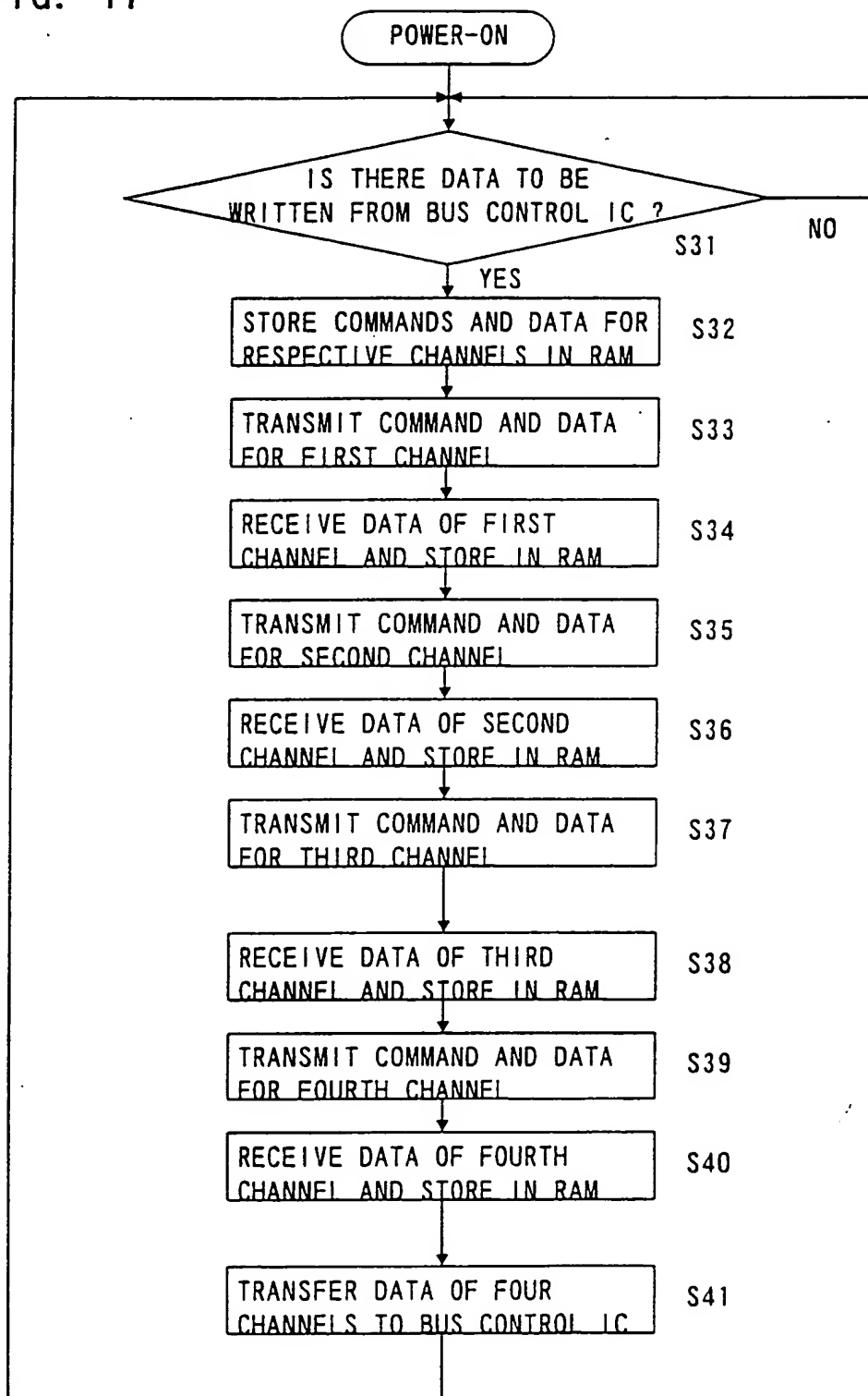
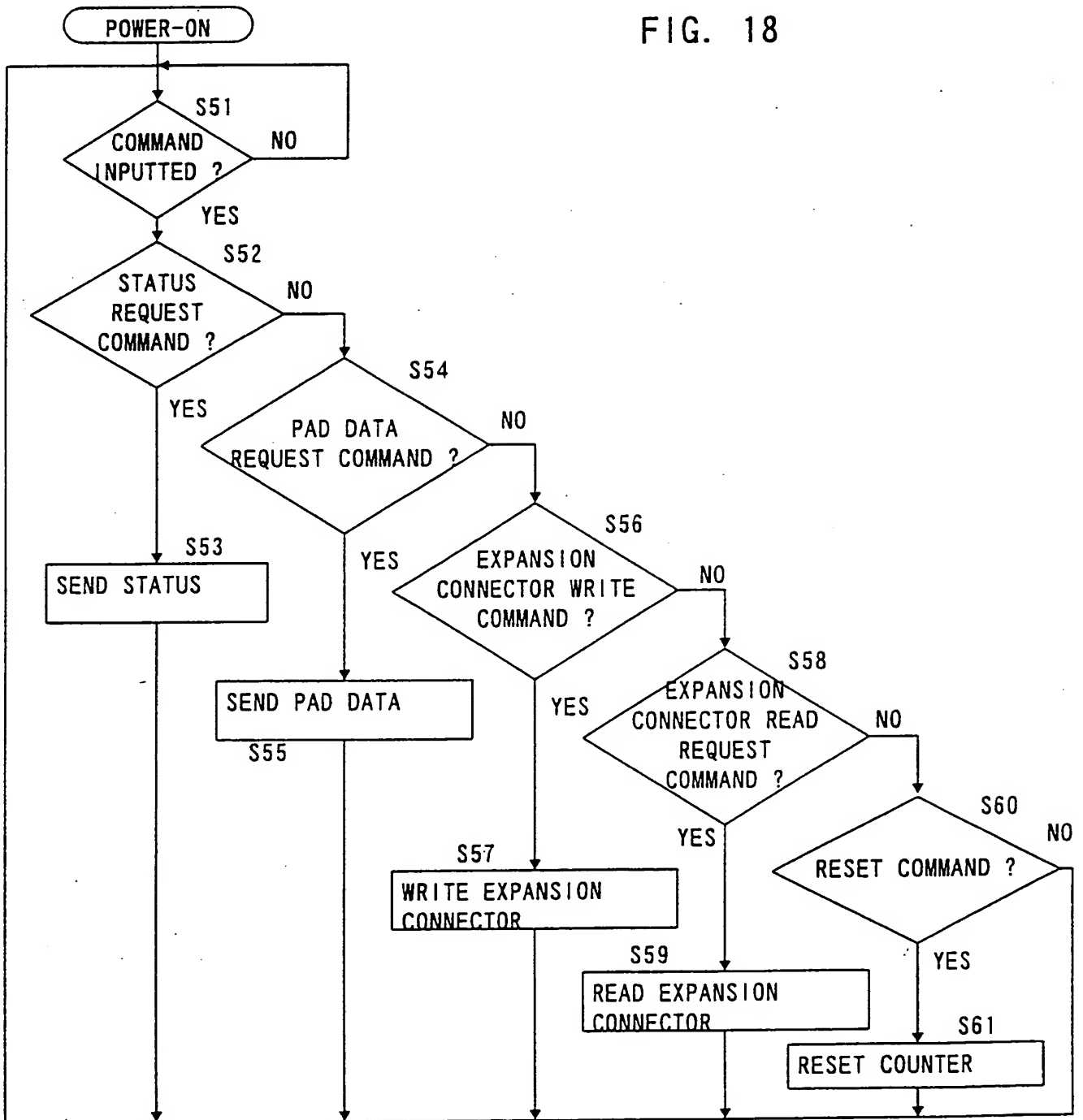


FIG. 18

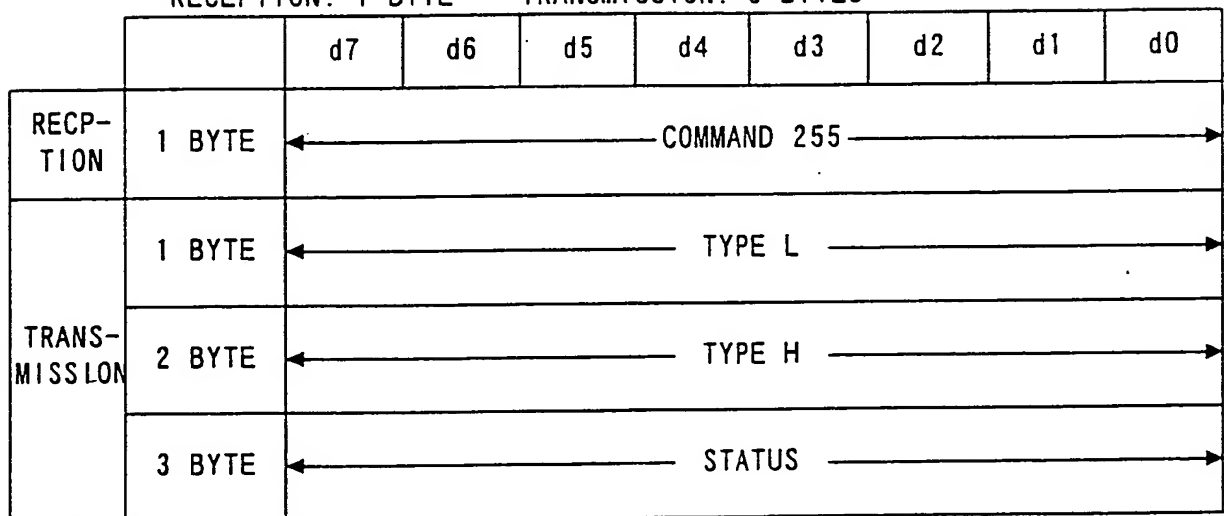




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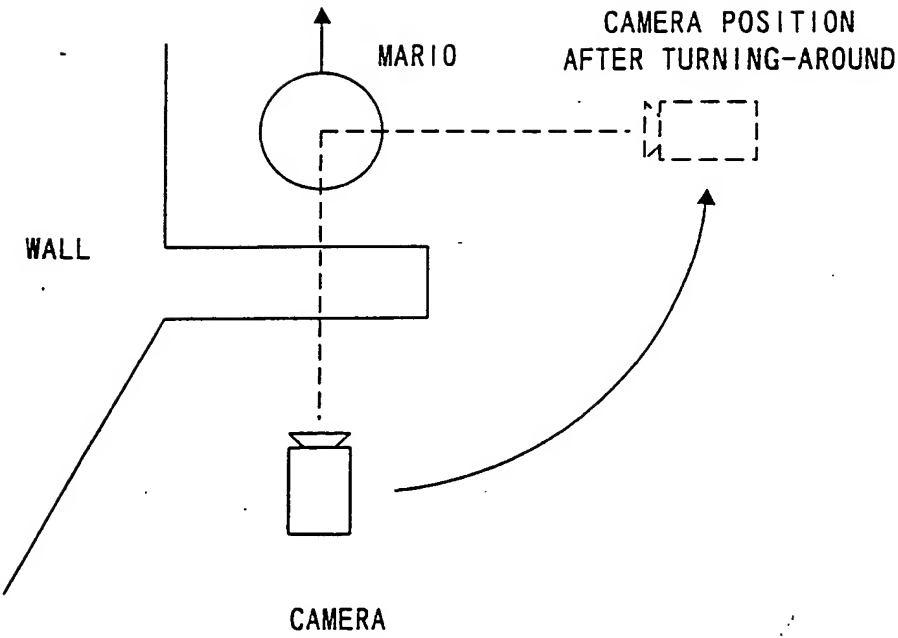
FIG. 19

COMMAND 255: CONTROLLER RESET  
 RECEPTION: 1 BYTE      TRANSMISSION: 3 BYTES



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FIG. 20



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FIG. 21

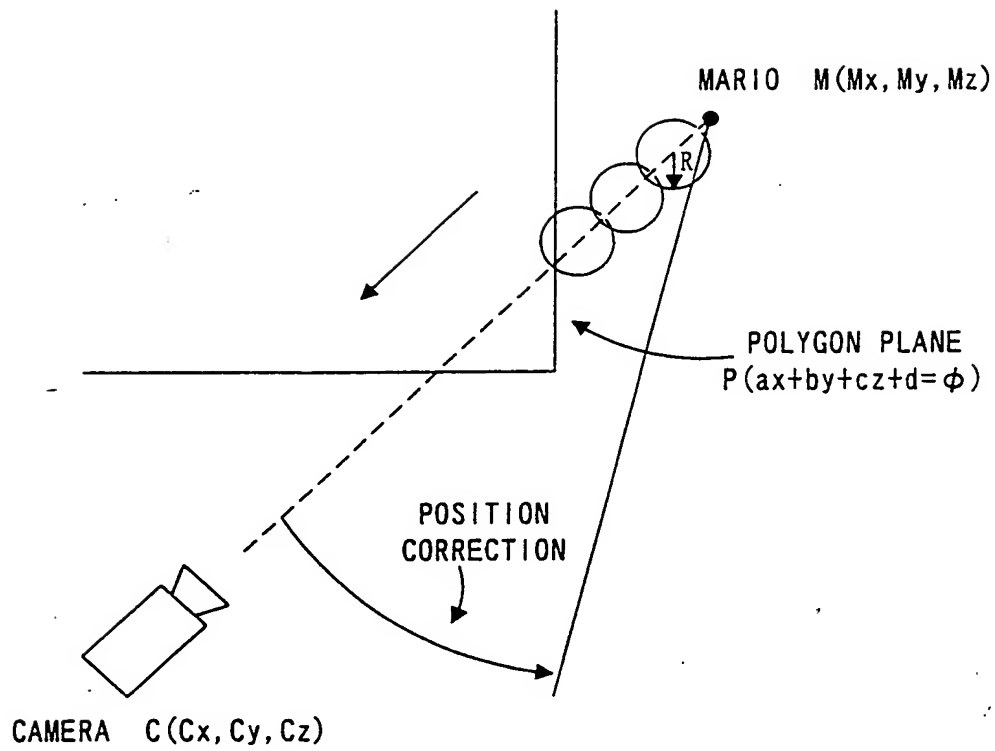
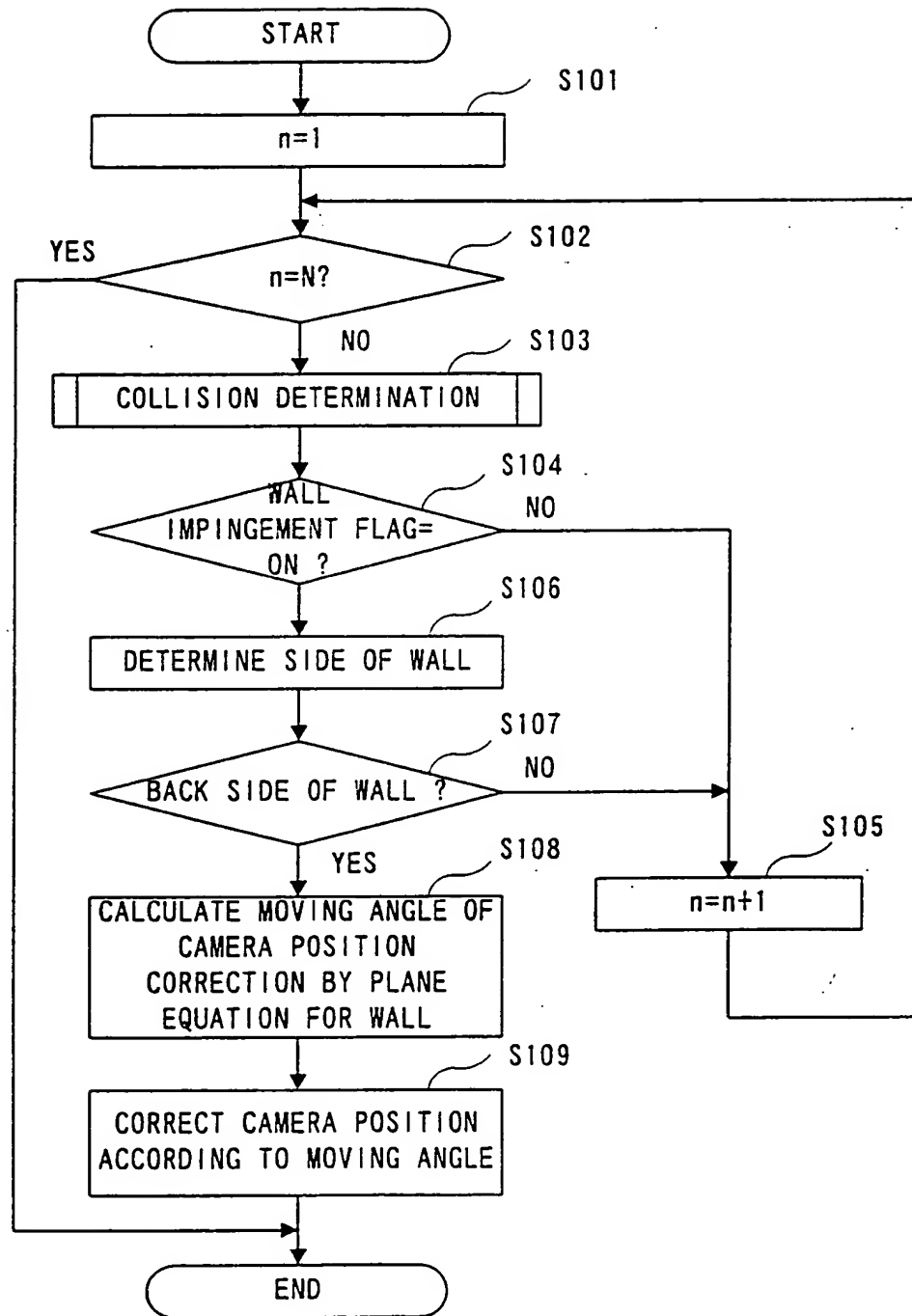
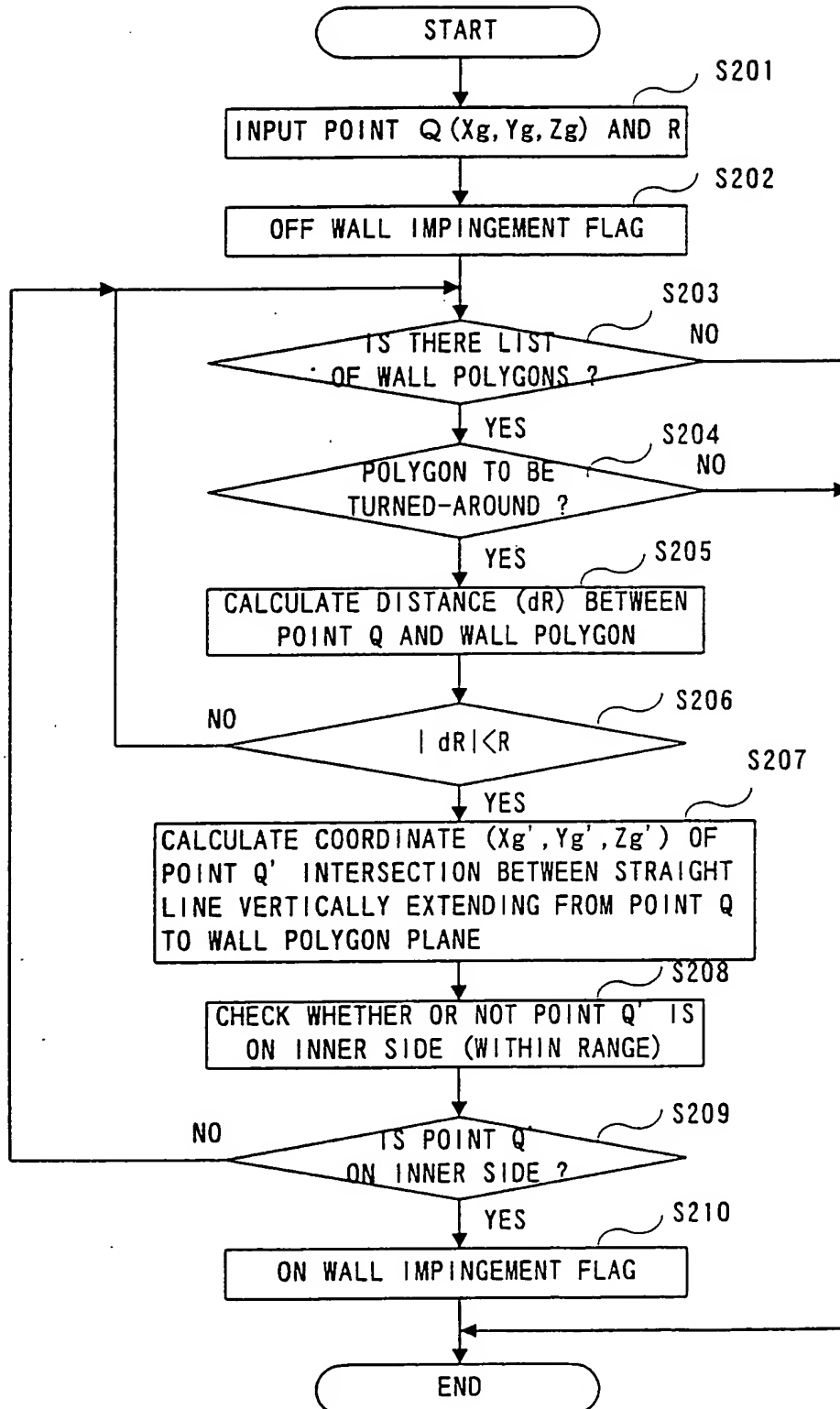


FIG. 22



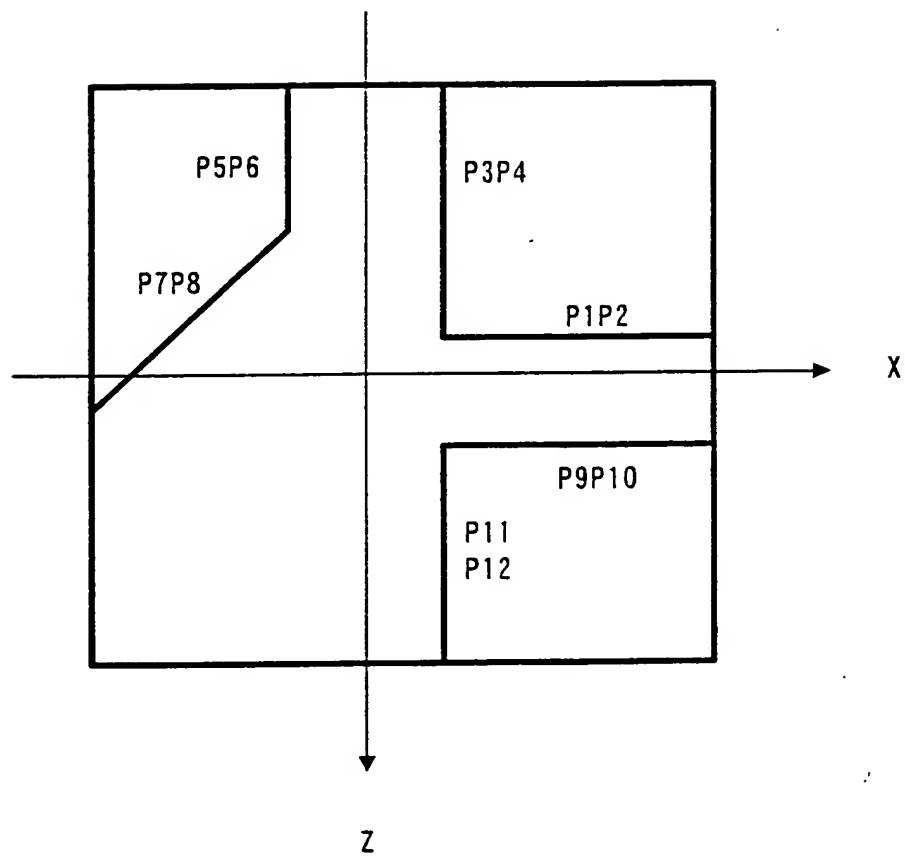
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FIG. 23



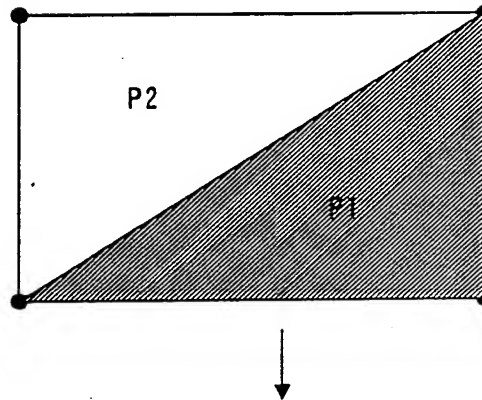
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FIG. 24



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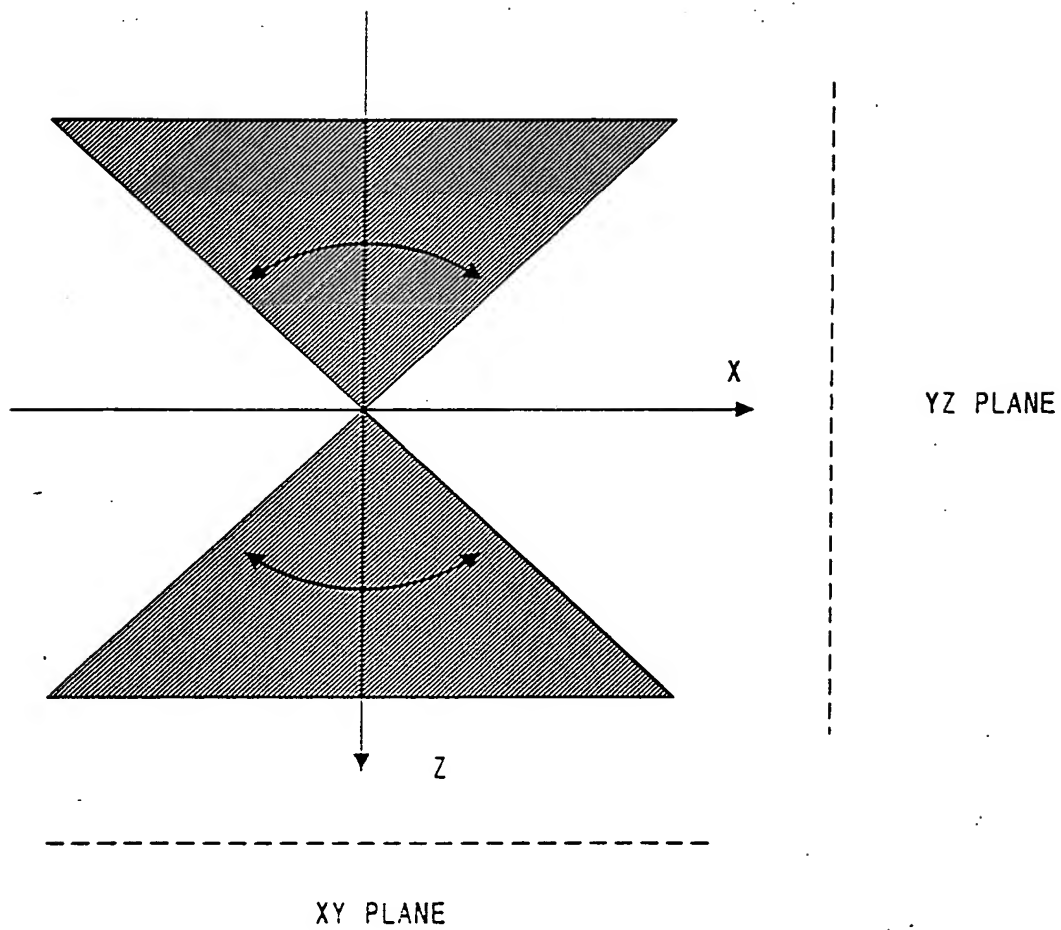
FIG. 25



TRIANGLE POLYGON

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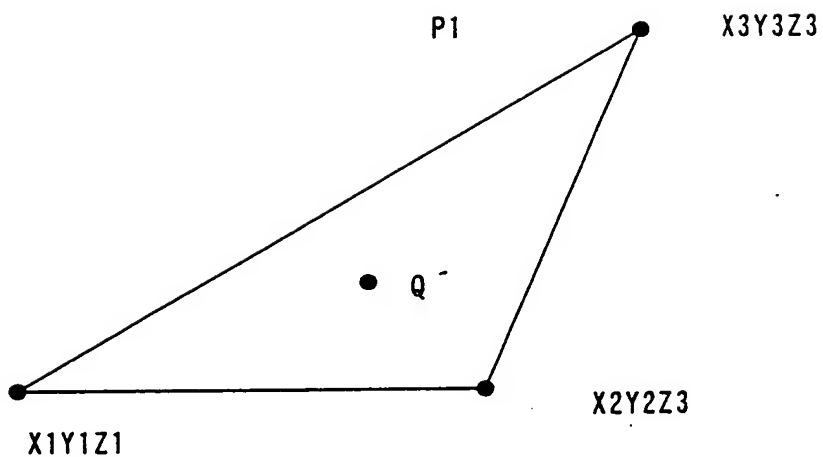
FIG. 26





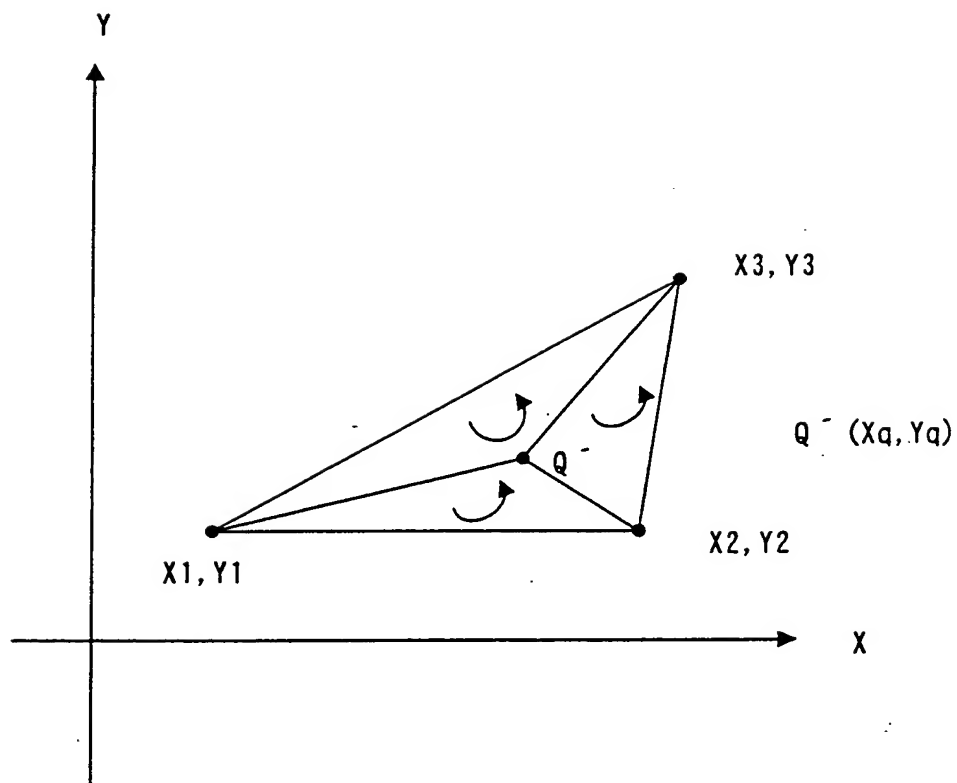
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FIG. 27



APPROVED	O.G. FIG.	
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FIG. 28



APPROVED	O.G. FIG.	
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FIG. 29

